Claims

1. (Original) A method to provide a triple well in an epitaxially based CMOS or BiCMOS process, comprising the step of implanting the triple well prior to the epitaxial deposition.

2. (Original) The method according to claim 1, comprising the step of using arsenic when implanting the triple well, wherein a slow diffusion will occur.

3. (Original) The method according to claim 2, comprising the step of adding at least one NMOS device in an achieved structure.

4. (Original) The method according to claim 2, comprising the step of implanting Boron prior to the epitaxial deposition.

5. (Original) The method according to claim 3, comprising the step of implanting Boron prior to the epitaxial deposition.

6. (Original) The method according to claim 4, comprising the step of adding more than one NMOS device in an achieved structure.

7. (Original) The method according to claim 5, comprising the step of adding more than one NMOS device in an achieved structure.

8. (Currently Amended) A method to provide a triple well in an epitaxially based CMOS or BiCMOS process, comprising the steps of:

- providing a semiconductor substrate;
- applying a first mask having openings only in areas for said triple well;
- applying an ion implant;
- applying a second mask having openings surrounding said ion implant;
- implanting a first <u>area</u>~~trench~~ surrounding said ion implant;
- depositing an epitaxial layer.

9. (Original) The method according to claim 8, wherein the ion implant is an arsenic ion implant.

10. (Original) The method according to claim 8, wherein a doping dose of $2x10^{13}$ cm^{-2}, energy of 480 keV and a tilt angle of 0 degree is used to penetrate deep into the substrate.

11. (Currently Amended) The method according to claim 8, further comprising the steps of:

- providing a third mask on top of said **substrate**~~epitaxial layer~~ before depositing said epitaxial layer, and

- implanting at least a second **area**~~trench~~.

12. (Currently Amended) The method according to claim 8, further comprising the step of etching said epitaxial layer to provide third **area**~~trenches~~ above said first **area**~~trenches~~.

13. (Currently Amended) The method according to claim 12, wherein the third **area**~~trenches~~ are filled by a dielectric material.

14. (Original) The method according to claim 13, wherein the dielectric material is a High Density Plasma oxide.

15. (Currently Amended) The method according to claim 11, further comprising the step of etching said epitaxial layer to provide third **area**~~trenches~~ above said first and second trenches.

16. (Currently Amended) The method according to claim 15, wherein the third **area**~~trenches~~ are filled by a dielectric material.

17. (Original) The method according to claim 16, wherein the dielectric material is a High Density Plasma oxide.

18. (Original) The method according to claim 12, further comprising the step of planarizing said epitaxial layer.

19. (Original) The method according to claim 18, wherein the planarizing is performed by chemical and/or mechanical polishing.

20. (Currently Amended) The method according to claim 8, wherein the substrate is of p-type and the triple well and first **area**~~trenches~~ are of n-type.